

### REMARKS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested. After entry of the foregoing amendment, Claims 1-7 and 9-12 remain pending in the present application. No new matter has been added.

By way of summary, the Official Action presents the following issues: the incorporation of Japanese Patent Application 2004-112318 by reference was indicated as improper; Claims 5-9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Vis (U.S. Patent No. 7,012,772 B1) in view of Fermo et al. (“Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers” (2000) (unpublished manuscript, on file with the Office), hereinafter “Fermo”) in view of Terrell et al. (Digital Signal Processing: Principals, Devices and Applications 86 (N. B. Jones & J. D. McK. Watson eds., Institution of Engineering and Technology 1990) (1982), hereinafter “Terrell”); and Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fermo in view of Terrell.

### FORM PTO-892

Applicant notes that the Form PTO-892 included with the Official Action does not cite Vis. Applicant respectfully requests that, because Vis has been cited in the rejections of Claims 1-9, the next Official Communication include Vis on a Form PTO-892.

### INCORPORATION BY REFERENCE

The Office has indicated that the incorporation of Japanese Patent Application 2004-112318 by reference was improper. Applicant respectfully traverses this indication, because the application clearly states that “The present invention contains subject matter related to

Japanese Patent Application JP 2004-112318 filed in the Japanese Patent Office on April 6, 2004, the entire contents of which are incorporated herein by reference.”<sup>1</sup> That is, the incorporation uses the words “incorporat(e)” and “reference,” and clearly identifies Japanese Patent Application JP 2004-112318. Accordingly, Applicant respectfully submits that the incorporation complies with 37 C.F.R. § 1.57(b).

Further, the Office has required Applicant to supply an English language translation of any prior-filed application that is in a language other than English. Applicants file herewith an accurate English translation of Japanese Patent Application JP 2004-112318 and a statement signed by the translator regarding the accuracy of the filed English translation. Accordingly, it is respectfully submitted that the requirement to supply an English language translation has been fulfilled.

#### REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fermo in view of Terrell.

In light of the rejection on the merits, independent Claims 1 and 4 have been amended to clarify the claimed invention and to thereby more clearly patentably define over the applied references.

Amended Claim 1 recites a signal processing apparatus, including, in part, a multiplication unit,

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<sup>1</sup> Spec., at 1.

said multiplication unit including,

one or more delay units . . . configured to delay a signal output from said multiplication unit, each by a unit time, [and]

a multiplier configured to multiply a signal output from said multiplication unit and a signal output from each of said one or more delay units, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every unit time . . . .

Applicant respectfully submits that Fermo in view of Terrell fail to disclose or suggest those features.

Fermo concerns an *Affine Projection* algorithm developed for a Simplified Volterra Filter structure.<sup>2</sup> Fermo does not describe a frequency with which the *Affine Projection* algorithm is applied.

It is respectfully submitted that Fermo is silent with regard to “one or more delay units . . . configured to delay a signal output from said multiplication unit, each by a unit time, . . . said multiplier being further configured to update each preset coefficient every unit time,” as recited in amended Claim 1.

Terrell concerns a Finite Impulse Response digital filter in which “the present output sample value is computed using a scaled version of the present input sample, and scaled versions of previous input samples.”<sup>3</sup> Terrell does not describe updating the scaling.

Applicant respectfully submits that Terrell fails to disclose or suggest “one or more delay units . . . configured to delay a signal output from said multiplication unit, each by a unit time, . . . said multiplier being further configured to update each preset coefficient every unit time,” as recited in amended Claim 1.

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<sup>2</sup> Fermo, at 2.

<sup>3</sup> Terrell.

Thus, it is submitted that Fermo and Terrell, taken alone or in combination, fail to disclose or suggest “one or more delay units . . . configured to delay a signal output from said multiplication unit, each by a unit time, . . . said multiplier being further configured to update each preset coefficient every unit time,” as recited in amended Claim 1. It is therefore submitted that independent Claim 1 (and all associated dependent claims) patentably distinguishes over any proper combination of Fermo and Terrell.

Applicant further submits that amended Claim 4 is allowable for the same reasons as discussed above with regard to Claim 1 and for the more detailed features presented in Claim 4.

Claims 5-9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Vis in view of Fermo and Terrell.

In light of the rejection on the merits, independent Claims 5 and 9 have been amended to clarify the claimed invention and to thereby more clearly patentably define over the applied references.

Amended Claim 5 recites a signal decoding apparatus, including, in part,

a processor . . . configured to detect an error, at a preset unit time, . . .

one or more series-connected delaying units configured to delay signals . . . each by the preset unit time, [and]

a multiplier configured to multiply a signal . . . and a signal . . . , each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time . . . .

Applicant respectfully submits that Vis, Fermo, and Terrell fail to disclose or suggest those features.

Vis concerns a circuit in which,

The coefficients for both the linear component  $H_1(z)$  12 and the non-linear component  $H_2(z_1, z_2)$  18 are updated by a least-mean-square (LMS) adaptation circuit 20 which adjusts the coefficients  $C$  36 and  $C_{n \times n}$  38 in a manner that minimizes the squared error  $e_k$  22 computed as the difference 28 between the sample values  $y_k$  32 output by the Volterra filter and estimated ideal sample values  $\hat{S}_k$  26 corresponding to the desired partial response.<sup>4</sup>

Further to Vis, “At every sample interval, the previous coefficients  $C$  and  $C_{n \times n}$  are loaded into the LMS update circuits 40 and 42, updated coefficients are computed, and the updated coefficients restored to the filters for use in generating the next output sample  $y_k$  32.”<sup>5</sup>

That is, Vis merely describes updating the coefficients at every sample interval. Vis does not further clarify the relationships held by the sample interval. It is submitted that Vis does not disclose or suggest “a processor . . . configured to detect an error, at a preset unit time, . . . one or more series-connected delaying units configured to delay signals . . . each by the preset unit time, [and] a multiplier configured to multiply a signal . . . and a signal . . . , each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time,” as recited in amended Claim 5.

Further, it is submitted that Fermo does not describe a frequency with which its *Affine Projection* algorithm is applied. It is also submitted that Terrell does not describe updating its scaling. It is therefore submitted that Fermo and Terrell fail to disclose or suggest “a processor . . . configured to detect an error, at a preset unit time, . . . one or more series-connected delaying units configured to delay signals . . . each by the preset unit time, [and] a multiplier configured to multiply a signal . . . and a signal . . . , each with a preset

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<sup>4</sup> Vis, col. 5, ll. 7-15.

<sup>5</sup> Id., ll. 59-63.

coefficient, said multiplier being further configured to update each preset coefficient every preset unit time,” as recited in amended Claim 5.

Thus, Vis, Fermo, and Terrell, taken alone or in combination, fail to disclose or suggest “a processor . . . configured to detect an error, at a preset unit time, . . . one or more series-connected delaying units configured to delay signals . . . each by the preset unit time, [and] a multiplier configured to multiply a signal . . . and a signal . . . , each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time,” as recited in amended Claim 5. It is respectfully submitted that independent Claim 5 (and all associated dependent claims) patentably distinguishes over any proper combination of Vis, Fermo, and Terrell.

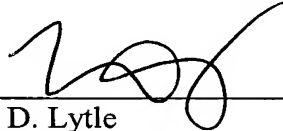
Further, it is submitted that amended Claim 9 is allowable for the same reasons as discussed with regard to Claim 5 and for the more detailed features presented in Claim 9.

CONCLUSION

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the present application, including Claims 1-7 and 9-12, is patentably distinguished over the cited art and is in condition for allowance. Such an allowance is respectfully requested at an early date.

Respectfully submitted,

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